SPECIFICATION AMENDMENT

Please replace the paragraph beginning at page 21, line 2, with the following rewritten paragraph:

The first selection circuit 205 receives the address signals CWA, CRA ~~CEA, CRE~~, EWA, ERA, and selects one of them in response to the logic level of the access request signal CWE, the output signal F2 and the output signal M2. The selected address signal are outputted to an address terminal A of the SP-RAM 201. In the memory control circuit 602, when the logic level of the access request signal CWE, the output signal F2 and the output signal M2 is at the L level, the address signal CWA is selected. When the logic level of the access request signal CWE is at the H level and the logic level of the output signals F2, M2 is the L level, the address signal CRA is selected. When the logic level of the output signal F2 is at the H level and the logic level of the output signal M2 and the access request signal CWE is the L level, the address signal ERA is selected. When the logic level of the output signal M2 is at the H level and the logic level of the output signal F2 and the access request signal CWE is the L level, the address signal EWA is selected.